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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,751	01/26/2004	Leonard C. Pipes	ITL.0851D1US (P15016D)	8763

7590 09/16/2004

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 09/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/764,751	PIPES ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 1/26/04. Currently, claims 15-20 are pending.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 16-20 are objected to because of the following informalities: On line 1 of each claim, respectively, "claim 14" should be "claim 15" so that each claim is dependent on claim 15, since claim 14 has been canceled. Therefore, for the purpose of examination on the merits, The Examiner will regard the limitation as "claim 15". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kamath et al., US Patent 6,569,739 in view of *Stanley Wolf, Silicon Processing For the VLSI Era, Volume II, Lattice Press, 1990, pages 21 and 45-48.*

Kamath discloses the apparatus substantially as claimed. See figures 1-8, and corresponding text, where Kamath shows, pertaining to claim 15, an apparatus comprising: a

semiconductor substrate **100** having a barrier layer **102** formed thereon (figures 1-4; col. 1, lines 58); a trench **101** etched into the substrate adjacent the barrier layer (figures 1-4; col. 37-49); and a plurality of ions **130** implanted into the dielectric layer (figure 5; col. 6, lines 22-40). In addition, Kamath shows, pertaining claim 16, the apparatus further comprising a plurality of ions implanted into the barrier (col.6, lines 35-40). In addition, Kamath shows, pertaining to claim 18, the apparatus wherein the dielectric layer comprises a silicon oxide layer (col. 5, lines 8-15). Also, Kamath shows, pertaining to claim 19, the apparatus wherein the dielectric layer is damaged by the plurality of implanted ions (figure 5; col. 6, lines 22-28). Finally, Kamath shows, pertaining to claim 20, the apparatus wherein the plurality of ions is selected from the group consisting of silicon, carbon, nitrogen, and oxygen (col. 7, lines 9-23, nitrogen).

However, Kamath fails to show, pertaining to claim 15, a dielectric layer deposited over the barrier layer and trench. In addition, Kamath fails to show, pertaining to claim 17, the apparatus wherein the barrier layer comprises a silicon nitride layer.

Wolf teaches, in figures 2-32(b), and pages 21 and 45-48, pertaining to claims 15 and 17, conventional techniques used to form a shallow trench refill with a CVD-SiO_2 and the use of a silicon nitride layer that will include an apparatus comprising a dielectric layer deposited over the barrier layer and the trench, or the barrier layer comprised of a silicon nitride layer.

It would have been obvious to one of ordinary skill in the art to incorporate into the apparatus of Kamath, a dielectric layer deposited over the barrier layer and the trench or, the barrier layer comprised of a silicon nitride layer, pertaining to claims 15 and 17, according to the teachings of Wolf, with the motivation that, conventional shallow trench isolation technology, includes a silicon oxide layer formed by chemical vapor deposition (CVD) being deposited onto

the surface of the wafer and then etched back to form a planar surface. In addition, a thick layer of CVD silicon nitride on the surface of the wafer prior to the CVD deposition functions as an oxidation mask used to prevent oxidizing species from reaching the silicon surface. Therefore, it would be obvious to one of ordinary skill in the art to use well known conventional techniques, which include an apparatus comprising a dielectric layer being deposited over the barrier layer and the trench, or the barrier layer made of silicon nitride, for the purpose of isolating semiconductor devices, as well as, protecting the trench surface within the silicon substrate from oxidation processing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
September 10, 2004

LYNNE A. GURLEY
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